AMENDMENTS TO THE CLAIMS:

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

CLAIMS 1-6 (Canceled).

7. (Currently Amended) An IC tag for transmitting first information to a reception unit, comprising:

a memory which memorizes the first information and second information to control the time of transmission of the first information to the reception unit; and

a memory address counter in which its count value indicates a bit address of the memory pertaining to the first information,

wherein the IC tag carries out count-up or count-down of a count value of the counter according to a clock signal received from the reception unit and the IC tag sets the second information stored in the memory as an initial value of the memory address counter and after the count value of the memory address counter reaches a specified code, the first information stored in the bit address indicated by the count value is sent out to the reception unit successively.

8. (Currently Amended) The IC tag according to claim 7,

wherein the memory memorizes ~~the~~ third information and the IC tag sets either the second information or the third information as an initial value of the memory address counter.

9. (Currently Amended) The IC tag according to claim 8, further comprising a mode switching portion,

wherein the IC tag selects the second information or the third information by means of the mode switching portion and sets it as an initial value of the memory address counter.

10. (Currently Amended) The IC tag according to claim 9,

wherein the mode switching portion is a flip-flop and the IC tag selects the second information or the third information according to a value of the flip-flop and sets it as an initial value of the memory address counter.

11. (Original) The IC tag according to claim 10,

wherein the specified code is zero.

12. (Currently Amended) The IC tag according to claim 10,

wherein the memory address counter and the second information have the same bit number.

13. (Previously Presented) The IC tag according to claim 10,

wherein the first information is comprised of at least an identification number and an error detection code for detecting an error in the identification number.

14. (Currently Amended) A reading method for reading first information from an IC tag having a memory which memorizes first information and second information to control the time of transmission of the first information to the reception

unit and a memory address counter in which a count value thereof indicates a bit address of the memory pertaining to the first information, comprising:

transmitting a clock signal from the reception unit to the IC tag;

setting the second information stored in the memory as an initial value of the memory address counter;

performing count-up or count-down of a count value of the memory address counter according to the clock signal; and

after the count value of the memory address counter reaches a specified code, transmitting the first information stored in the bit address indicated with the count value successively to the reception unit.

15. (Currently Amended) The reading method according to claim 14,

wherein the memory memorizes ~~the~~ third information and the second information is selected according to the mode switching signal and set up in the IC tag as an initial value of the memory address counter.

16. (Original) The IC tag according to claim 8,

wherein the specified code is zero.

17. (Original) The IC tag according to claim 9,

wherein the specified code is zero.

18. (Currently Amended) The reading method according to claim 14,

wherein the specified code is zero.

19. (Currently Amended) The IC tag according to claim 8,

wherein the memory address counter and the second ~~memory~~ information have the same bit number.

20. (Currently Amended) The IC tag according to claim 9,

wherein the memory address counter and the second ~~memory~~ information have the same bit number.

21. (Currently Amended) The reading method according to claim 14,

wherein the memory address counter and the second ~~memory~~ information have the same bit number.

22. (Previously Presented) The IC tag according to claim 8,

wherein the first information is comprised of at least an identification number and an error detection code for detecting an error in the identification number; and

wherein the second information is a random number.

23. (Previously Presented) The IC tag according to claim 9,

wherein the first information is comprised of at least an identification number and an error detection code for detecting an error in the identification number.

24. (Previously Presented) The reading method according to claim 14,

wherein the first information is comprised of at least an identification number and an error detection code for detecting an error in the identification number; and

wherein the second information is a random number.

25. (New) The IC tag according to claim 7,
wherein said second information is a random number.

26. (New) The reading method according to claim 14,
wherein said second information is a random number.

27. (New) The IC tag according to claim 7,
wherein the first information identifies the IC tag.

28. (New) The IC tag according to claim 25,
wherein the first information identifies the IC tag.

29. (New) The reading method according to claim 14,
wherein the first information identifies the IC tag.

30. (New) The reading method according to claim 26,
wherein the first information identifies the IC tag.